

Serial No.: 10/796,426	Confirmation No.: 1895	Art Unit: 2183
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors:	Brian Robert Prasky	Date:	12 June 2009
Serial No.:	10/796,426	Art Unit:	2183
Filing Date:	9 March 2004	Examiner:	Brian P. Johnson
Confirmation No.:	1895	Docket No.:	POU920030068US1
Title:	Method, System and Program Product for a Pipelined Processor Having a Branch Target Buffer (BTB) Table with a Recent Entry Queue in Parallel with the BTB Table	Attorney:	Graham S. Jones, II 42 Barnard Avenue Poughkeepsie, NY 12603-5023

REQUEST FOR CORRECTION OF SPELLING OF TITLE

**The Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450**

Your Honor:

In response to the Office Action of March 13, 2009, please amend the above-identified application as follows:

**Correction of Title in PAIR begins on page 2 of this paper.
Remarks/Arguments begin on page 3 of this paper.**